Module 5

DC to AC Converters

Lesson 36

3-Phase Pulse Width Modulated (PWM) Inverter

After completion of this lesson the reader will be able to:

(i) Explain the philosophy behind PWM inverters.
(ii) Understand the advantages and disadvantages of PWM inverters.
(iii) Compare the quality of output voltage produced by different PWM inverters
(iv) Decide on voltage and current ratings of inverter switches.

Pulse width modulated (PWM) inverters are among the most used power-electronic circuits in practical applications. These inverters are capable of producing ac voltages of variable magnitude as well as variable frequency. The quality of output voltage can also be greatly enhanced, when compared with those of square wave inverters discussed in Lesson-35. The PWM inverters are very commonly used in adjustable speed ac motor drive loads where one needs to feed the motor with variable voltage, variable frequency supply. For wide variation in drive speed, the frequency of the applied ac voltage needs to be varied over a wide range. The applied voltage also needs to vary almost linearly with the frequency. PWM inverters can be of single phase as well as three phase types. Their principle of operation remains similar and hence in this lesson the emphasis has been put on the more general, 3-phase type PWM inverter.

There are several different PWM techniques, differing in their methods of implementation. However in all these techniques the aim is to generate an output voltage, which after some filtering, would result in a good quality sinusoidal voltage waveform of desired fundamental frequency and magnitude. As will be discussed later in this chapter, for the inverter topology considered here, it may not be possible to reduce the overall voltage distortion due to harmonics but by proper switching control the magnitudes of lower order harmonic voltages can be reduced, often at the cost of increasing the magnitudes of higher order harmonic voltages. Such a situation is acceptable in most cases as the harmonic voltages of higher frequencies can be satisfactorily filtered using lower sizes of filter chokes and capacitors. Many of the loads, like motor loads have an inherent quality to suppress high frequency harmonic currents and hence an external filter may not be necessary.

To judge the quality of voltage produced by a PWM inverter, a detailed harmonic analysis of the voltage waveform needs to be done. In the following discussions some of the results of harmonic analysis done in the previous lessons have been borrowed. In Lesson-35, while discussing the 3-phase square wave inverter it was shown that the magnitudes of fundamental components of the inverter pole voltage (voltage between the output of an inverter leg and the mid potential point of the input dc supply) and the load phase voltage are identical provided the load is a balanced 3-phase load. In fact, after removing 3^{rd} and multiples of 3^{rd} harmonics from the pole voltage waveform one obtains the corresponding load phase voltage waveform. The pole voltage waveforms of 3-phase inverter are simpler to visualize and analyze and hence in this lesson the harmonic analysis of load phase and line voltage waveforms is done via the harmonic analysis of the pole voltages. It is implicit that the load phase and line voltages will not be affected by the 3^{rd} and multiples of 3^{rd} harmonic components that may be present in the pole voltage waveforms.

36.1 Nature Of Pole Voltage Waveforms Output By PWM Inverters

Unlike in square wave inverters the switches of PWM inverters are turned on and off at significantly higher frequencies than the fundamental frequency of the output voltage waveform. The typical pole voltage waveform of a PWM inverter is shown in Fig. 36.1 over one cycle of output voltage. In a three-phase inverter the other two pole voltages have identical shapes but they are displaced in time by one third of an output cycle. Compared to the square pole voltage waveform seen in Lesson-35, the pole voltage waveform of the PWM inverter changes polarity several times during each half cycle. The time instances at which the voltage polarities reverse have been referred here as notch angles. It may be noted that the instantaneous magnitude of pole voltage waveform remains fixed at half the input dc voltage (E_{dc}). When upper switch (S_U), connected to the positive dc bus is on, the pole voltage is + 0.5 E_{dc} and when the lower switch (S_L), connected to the negative dc bus, is on the instantaneous pole voltage is - 0.5 E_{dc}. The switching transition time has been neglected in accordance with the assumption of ideal switches. It is to be remembered that in voltage source inverters, meant to feed an inductive type load, the upper and lower switches of the inverter pole conduct in a complementary manner. That is, when upper switch is on the lower is off and vice-versa. Both upper and lower switches

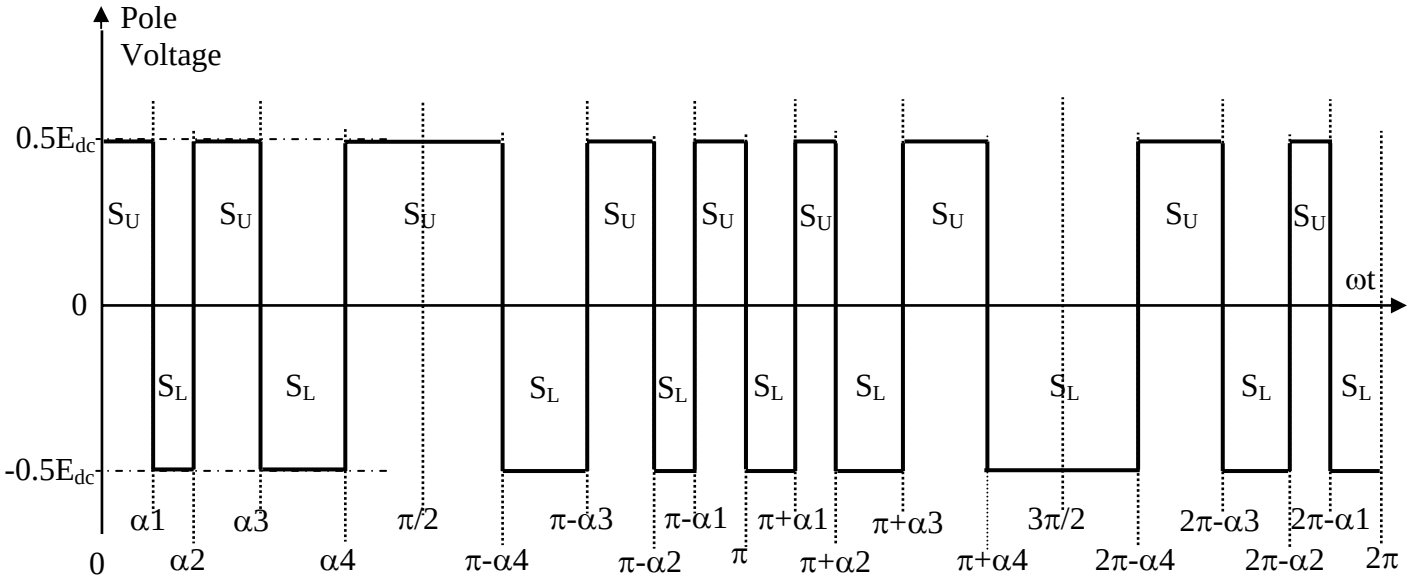

Fig.36.1: A typical pole-voltage waveform of a PWM inverter

should not remain on simultaneously as this will cause short circuit across the dc bus. On the other hand one of these two switches in each pole (leg) must always conduct to provide continuity of current through inductive loads. A sudden disruption in inductive load current will cause a large voltage spike that may damage the inverter circuit and the load.

36.2 Harmonic Analysis Of Pole Voltage Waveform

The pole voltage waveform shown in Fig. 36.1 has half wave odd symmetry and quarter-wave mirror symmetry. The half wave odd symmetry of any repetitive waveform f(ωt), repeating after every 2π/ω duration, is defined by f(ωt) = - f(π+ωt). Such a symmetry in the waveform amounts

to absence of dc and even harmonic components from the waveform. All inverter output voltages maintain half wave odd symmetry to eliminate the unwanted dc voltage and the even harmonics. The half wave odd symmetry followed by quarter wave mirror symmetry, defined by f(ωt) = f(π-ωt), results in presence of only sine components in the Fourier series representation of the waveform. It may be verified that quarter wave symmetry may not hold good once the time origin is shifted arbitrarily. However the half-wave odd symmetry is maintained in spite of shifting of time origin. This is quite expected, as by just shifting the time origin new (even) harmonic frequencies will not creep up in the voltage waveform, whereas by shifting time origin the sine wave may become cosine or may have some other phase-shift. The quarter wave symmetry talked above is not necessary for improvement of the output waveform quality; it merely simplifies the Fourier analysis of the pole voltage waveform. It may also be noted that the quarter wave symmetry is not achieved at the cost of compromising the inverter's output capability (in terms of magnitude and quality of achievable output voltage).

With the assumed quarter wave mirror symmetry and half wave odd symmetry the waveform shown in Fig. 36.1 may be decomposed in terms of its Fourier components as below:-

$$V_{AO} = \sum_{n=1,3,5,....\infty} b_n \sin n\omega t \quad \text{.....(36.1)}$$

where V_{AO} is the instantaneous magnitude of the pole voltage shown in Fig. 36.1 and b_n is the peak magnitude of its nth harmonic component. Because of the half wave and quarter wave symmetry of the waveform, mentioned before, the pole voltage has only odd harmonics and has only sinusoidal components in the Fourier expansion. Thus the pole voltage will have fundamental, third, fifth, seventh, ninth, eleventh and other odd harmonics. The peak magnitude of nth harmonic voltage is given as:

$$b_n = \frac{2E}{n\pi}(1 - 2\cos n\alpha_1 + 2\cos n\alpha_2 - 2\cos n\alpha_3 + 2\cos n\alpha_4) \text{.....(36.2)}$$

, where α_1, α_2, α_3 and α_4 are the four notch angles in the quarter cycle ($0 \le \omega t \le \pi/2$) of the waveform.

Now, as described in the beginning of this lesson, the third and multiples of third harmonics do not show up in the load phase and line voltage waveforms of a balanced 3-phase load. Most of the three phase loads of interest are of balanced type and for such loads one need not worry about triplen (3rd and multiples of 3rd) harmonic distortion of the pole voltages. The peak magnitudes of fundamental (b_1) and three other lowest order harmonic voltages that matter most to the load can be written as:

$$b_1 = \frac{2E}{\pi}(1 - 2\cos\alpha_1 + 2\cos\alpha_2 - 2\cos\alpha_3 + 2\cos\alpha_4) \text{.....(36.3)}$$

$$b_5 = \frac{2E}{5\pi}(1 - 2\cos 5\alpha_1 + 2\cos 5\alpha_2 - 2\cos 5\alpha_3 + 2\cos 5\alpha_4) \text{.....(36.4)}$$

$$b_7 = \frac{2E}{5\pi}(1 - 2\cos 7\alpha_1 + 2\cos 7\alpha_2 - 2\cos 7\alpha_3 + 2\cos 7\alpha_4) \text{.....(36.5)}$$

$$b_{11} = \frac{2E}{11\pi}(1 - 2\cos 11\alpha_1 + 2\cos 11\alpha_2 - 2\cos 11\alpha_3 + 2\cos 11\alpha_4) \text{.....(36.6)}$$

It can be seen that the 3rd and 9th harmonics have been not considered, as they will not appear in the load side phase and line voltages. Most of the industrial loads are inductive in nature with an

inherent quality to attenuate currents due to higher order harmonic voltages. Thus after fundamental voltage, the other significant voltages for the load are 5^{th}, 7^{th} and 11^{th} etc.

Generally, only the fundamental frequency component in the output voltage is of interest and all other harmonic voltages are undesirable. As such one would like to eliminate as many low order harmonics as possible. Accordingly the fundamental voltage magnitude (b_1) may be set at the desired value and the magnitudes of fifth (b_5), seventh (b_7) and eleventh (b_{11}) harmonics may be set to zero. These voltage magnitudes when substituted in the expressions given by Eqns. 36.3 to 36.6 will lead to the solutions of the notch angles. One may like to eliminate many more unwanted harmonic frequencies from the load voltage waveform but this will require introduction of more notch angles per quarter cycle of the pole voltage. In fact if there are 'k' notch angles per quarter cycle, 'k' number of equations may be written each of which determines the magnitude of a particular harmonic voltage. Now, each time a notch angle is encountered in the pole voltage waveform, the top and bottom switches of that particular pole undergo a switching transition (on to off or vice versa). The switching frequency (f_{sw}) of the inverter switches can be equated to

$$f_{sw} = 2\ k\ f_1 \qquad \text{……...……...…….....(36.7)}$$

, where one turn-on and one turn-off has been taken as one switching cycle, 'k' is the number of notches per quarter cycle and f_1 is the frequency of fundamental component in the output voltage. Thus it can be seen that a better quality output waveform (in terms of elimination of more numbers of unwanted harmonic voltages) comes at the cost of increasing the switching frequency of the inverter. The switching frequency is directly proportional to the switching losses in the inverter switches. Also, the switch must be capable of being switched on and off at the required frequency. The IGBT switches used in medium power inverters are generally switched at a frequency of 20 kHz or more. With a switching frequency of 20 kHz and the output (fundamental) frequency of 50 Hz there will be up to 200 notches per quarter cycle of the output waveform. The load voltage can thus be made virtually free of low order harmonics and the load current (for an inductive load) can be expected to have a good quality sinusoidal waveform. The switching frequency of 20 kHz is important in another sense too. The range of audible noise for human beings extends from few Hertz to 20 kHz. Thus if the switching frequency is 20 kHz or beyond, the switching frequency related audible noise will not be present when the inverter operates. The inverter operation can then be very quite. If the inverter operates at low frequency, the connecting wires to the switches etc. also carry low frequency current producing low frequency vibrations (due to interaction of current with the stray magnetic field produced by other conductors etc.) and result in audible noise. Similarly low frequency current through inductors and transformers also produce audible noise. The humming or whistling type noise due to low switching frequency may at times be too annoying and unacceptable.

36.3 Trade Off Between Low Order And High Order Harmonics

The 3-phase inverter with six switches connected in the bridge fashion is also known as a two-level inverter because the inverter pole-voltage alternates between the two voltage levels of +0.5 E_{dc} and - 0.5 E_{dc} (the switching transition time has been neglected). The root mean square (rms) of the pole voltage equals 0.5 E_{dc}. Now a periodic function ' $f(\omega t)$ ' when expressed in terms of its Fourier components satisfies the following mathematical identity.

$$\left[f(\omega t)_{rms} \right]^2 = \left[f(\omega t)_{1,rms} \right]^2 + \sum_{n=2,3,4,....,\infty} \left[f(\omega t)_{n,rms} \right]^2 \quad \text{.....(36.8)}$$

In Eqn. (36.8), $f(\omega t)_{rms}$ is the rms magnitude of the given periodic waveform where as $f(\omega t)_{1,rms}$ and $f(\omega t)_{n,rms}$ are the rms magnitudes of the fundamental component and n^{th} harmonic component of the waveform respectively.

Also, if the waveform ' $f(\omega t)$ ' has half wave odd symmetry and quarter wave mirror symmetry, its fundamental voltage can be expressed as

$$f(\omega t)_{1,rms} = \frac{\sqrt{2}}{\pi} \int_{\omega t=0}^{\pi} \{ f(\omega t) \sin \omega t \} d\omega t \quad \text{.....(36.9)}$$

Now let $f(\omega t)$ in the above equations (36.8 and 36.9) be replaced by the two-level pole voltage waveform of the PWM inverter. The term on the left hand side of Eqn. (36.8) equals $(0.5E_{dc})^2$. The first term on the right hand side of Eqn. (36.8) is the square-of-rms (i.e., mean of square) magnitude of the fundamental component of pole voltage whereas the second term on the right hand side denotes the mean-of-square magnitude of the unwanted ripple in the pole voltage. As can be seen, the rms magnitude of the fundamental pole voltage is always going to be less than $0.5E_{dc}$. Further, as given by Eqn. (36.9), the fundamental magnitude (rms) of PWM inverter's output pole-voltage will be less than $0.45E_{dc}$, which is the rms magnitude of fundamental pole voltage of a 3-phase square wave inverter. [In case of square wave output, both $f(\omega t)$ and $\sin \omega t$ are positive during $0 \le \omega t \le \pi$ but the sign of $f(\omega t)$ in PWM waveform alternates between positive and negative values.]

In case of PWM inverter the magnitude of fundamental output voltage is fixed by suitable pulse width modulation (by selection of suitable notch angles for the waveform in Fig. 36.1). However, as can be seen from Eqn. (36.8), the reduction in fundamental magnitude leads to increase in the rms magnitude of the unwanted ripple voltage. Also, after fixing the fundamental voltage magnitude if it is desired to eliminate some of the low order harmonics, it will be at the cost of increasing the magnitudes of higher order harmonics. Thus, as far as the quality of inverter pole voltage alone is concerned the PWM technique is not helping. However considering the fact that most of the loads are inductive in nature with low pass filter type characteristics the load current quality effectively improves by eliminating lower order harmonics from the pole voltage waveform (even if the higher order harmonic magnitudes increase). In case the load, on its own, is not able to filter out the harmonic voltages satisfactorily the inverter output may be passed through some external filter before being applied to load. The required size of the external filter will be small if the inverter output is free from low frequency harmonics.

36.4 Brief Description Of Some Popular PWM Techniques

The schematic PWM waveform shown in Fig. 36.1, is only representative in nature. The logic described to select notch angles is also specific to one particular PWM technique that is known as selective harmonic elimination technique. There are several other PWM techniques, the important ones are:- SINE-PWM technique, Space Vector based PWM technique, Hysteresis current controller based PWM technique etc. A few of these techniques have been dealt with, in detail in the next few lessons.

Some of the PWM techniques can be realized using analog circuits alone; some others are more easily realized with the help of digital processors like microprocessor, Digital signal processor (DSP) or Personal Computer (PC), whereas some other PWM controllers could be a hybrid between analog and digital circuits. For example, the selective harmonic elimination technique described above requires numerical solutions of the transcendental equations for arriving at the required notch angles. These transcendental equations are solved off-line and the information regarding notch angles (switching instances) is stored in digital memory, like EPROM. It may be realized that the notch instances may not occur at regular time intervals. Similarly fundamental output voltage requirement may not remain fixed for all output frequencies and hence the transcendental equations (similar to Eqns. 36.3 to 36.6) will be different for different output frequencies. Also, as per Eqn. 36.7, if the switching frequency is kept constant, there will be more notch angles (per quarter cycle) at low output frequencies and less number of notches at higher frequencies. Thus the set of notch angles for one frequency may be different from the notch angles at some other frequency. For satisfactory implementation of this technique, generally the desired output frequency range is divided in few discrete frequencies. For example, it may be desired to output a 3-phase balanced voltage in the frequency range of 5 Hz to 50 Hz with the constraint that the ratio between output voltage magnitude and output frequency should remain fixed to some predetermined value. Under this situation the output voltage range may be discretized in steps of, say, 1Hz. Thus the available output may vary from 5 Hz to 50 Hz through the following discrete values of intermediate frequencies: 6 Hz, 7 Hz, 8 Hz, …, 49 Hz. The desired magnitudes of output voltage for all these discrete frequencies is found out and accordingly the notch angles are calculated to eliminate as many unwanted harmonics as possible (keeping in mind the constraint on switching frequency). Now switching information for successive output frequencies may be stored in successive memory blocks. For each of these output frequencies, it may be convenient to discretize one complete output cycle time interval in small steps (say, in steps of 10 microseconds) and the inverter switching word (as described below) at these successive time intervals are then stored in the successive memory locations. The switching word combines the switching information for all three legs (all six switches) of the inverter and may be obtained in the form of a six bit binary word, each bit corresponding to one particular switch. When a particular bit value is ‘1’ that particular switch may require being turned-on. Similarly ‘0’ bit value may correspond to turn-off command of the switch. Now if the memory block, containing switching information is addressed sequentially after every 10 microsecond (this being the time step, chosen above, to discretize the output cycle time period) the desired switching pattern for the inverter switches may be obtained. The notch angles can thus be realized with a maximum time error of 10 microseconds (which for 50 Hz output corresponds to an error of 0.18^0 only). After completion of one output cycle the next cycle is simply repeated like the previous one. One may move from one memory block to another memory block (by suitably multiplexing the memory address-word) to obtain the inverter-switching pattern for some other output frequency. The selective harmonic elimination technique described above is also known as stored-PWM technique. The overall memory requirement may be large but since the memory cost has been reducing over the years the stored-PWM technique remains one of the most attractive techniques.

In contrast to the selective harmonic elimination technique discussed above, some other PWM techniques, notably SINE-PWM and Space Vector-PWM techniques, try to match the mean value of load voltage under the rectangular PWM waveform with the mean voltage of the desired output waveform over every small time interval of the output cycle. If, for example, the desired output voltage is a sinusoidal waveform of a given magnitude and of frequency ‘f_1’, then for

every small time interval ‘Δt’ of the output cycle period (such that Δt << 1/ f_1) the mean (dc) magnitude under desired sine wave and the mean dc voltage under the PWM pulses are made equal. Now barring the mismatch in the instantaneous magnitudes of the sine wave and the PWM wave within the small time period ‘Δt’, the two waveforms are matching. Thus the PWM waveform may be considered to be the superposition of the desired output waveform and ripple voltages of time period Δt. The ripple voltage waveform in each ‘Δt’ time interval may not be identical and hence ripple voltage may consist of a band of harmonics of high frequency. In the frequency axis the high frequency harmonic voltages are far away from the desired voltage of fundamental frequency ‘f_1’ and hence suitable low pass filter circuits may be used to block the unwanted harmonic currents without affecting the magnitude of the fundamental frequency current. Further details of these techniques may be found in later lessons.

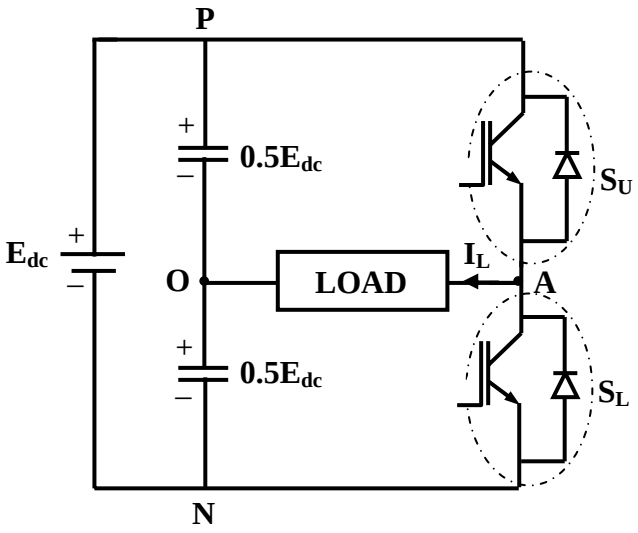

Fig. 36.2: 1-phase half bridge VSI for CCPWM control

Another popular PWM technique is current controlled PWM (CCPWM) technique. Here the instantaneous magnitude of load current is directly controlled, within some tolerable error band, to match the desired current shape. This technique is described below for a single-phase half bridge inverter shown in Fig.36.2. The positive sense for the load current (I_L) is taken along the direction of arrow in Fig. 36.2. The actual load current is sensed with the help of a current sensor and compared with its reference magnitude. The error in load current can be controlled, as described below, by proper switching of the inverter switches. The load could be a R-L load or a R-L-E load. In case of R-L-E load, it is assumed that the back emf (E) of the load has a peak magnitude lower than the magnitude of instantaneous pole voltage ($0.5E_{dc}$). To increase the actual current along the direction of arrow (or to reduce the current flowing in a direction opposite to the arrow) upper switch ‘S_U’ needs to be turned on, whereas turning on of lower switch ‘S_L’ will produce the reverse effect. This can be verified simply by writing and analyzing the loop voltage equation.

36.5 Two-Level Versus Three-Level PWM Inverters

As described in section 36.3, the three-phase bridge inverter consisting of six switches (shown in Lesson-35) can output pole voltages of only two levels $+0.5E_{dc}$ and $-0.5E_{dc}$. In contrast to a two-level inverter, a three-level inverter is capable of producing three different pole-voltage levels, namely, $+0.5E_{dc}$, zero and $-0.5E_{dc}$. The circuit details of three-level inverter will not be discussed

in this course but it can easily be shown that the three-level inverter will have better harmonic spectrum in comparison to the two-level inverter. As described by Eqn. (36.8) in section 36.3, any reduction in the fundamental output voltage magnitude of a two level inverter results in increased rms magnitude of unwanted ripple in the output waveform. Now, let Eqn. (36.8) be considered in relation to a three-level inverter. Since the pole voltage can now have zero level too, the rms magnitude of the pole voltage can be brought below $0.5E_{dc}$. For lower magnitude of fundamental pole-voltage, as given by Eqn. (36.9), suitable intervals of zero voltage level may be introduced such that with lowering of fundamental voltage the rms of the overall pole voltage also reduces. Thus the rms of the ripple voltage, in case of three-level inverter, can be made lower than that of the two-level inverter.

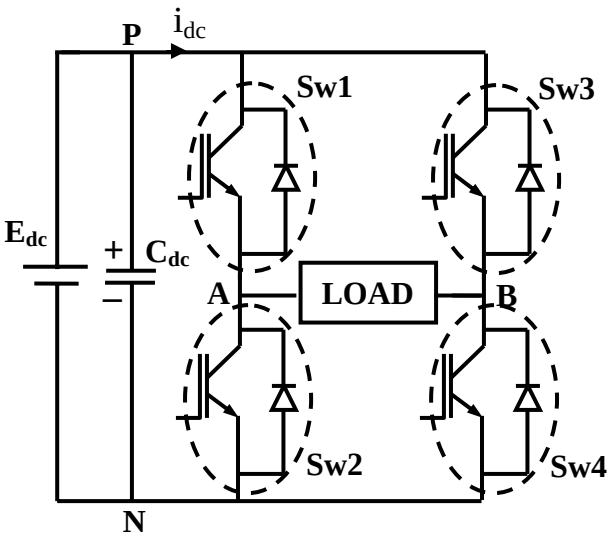

Fig. 36.3: A 1-phase full-bridge VSI

The three-level versus two-level comparison can be applicable to a single-phase PWM inverter too. Consider the single-phase full bridge circuit shown in Fig.36.3. For this circuit if all the time one of the two diagonal pair of switches, (Sw1 and Sw4) or (Sw2 and Sw3), conduct the load voltage will have two levels; +E or –E. By suitably switching between one diagonal pair to another diagonal pair one can obtain a PWM waveform similar to the pole voltage waveform of a three-phase PWM inverter (only change is in the voltage magnitude). Now if the allowed switching combination includes conduction of Sw1 along with Sw3 (or Sw2 along with Sw4) the load voltage may have three-levels, i.e., +E, zero and –E. As with a three-phase inverter, the single phase PWM inverter too will have lower voltage distortion in case of three-level load voltage (than the corresponding distortion in two level output).

36.6 Considerations On Switch Voltage And Current Ratings

As in square wave inverter the switches of PWM inverter must also be rated for the maximum dc link voltage. There will, however, be a significant difference in the switch current ratings of the square wave and PWM inverter for comparable magnitudes of inverters' output current. This is due to the increased switching losses in the PWM inverter. Since the switches in PWM inverter operate at much higher frequencies than in square wave inverter, the switching losses in the former are comparable to the conduction losses. This calls for suitable de-rating of the switch current rating. For medium power rated inverters mostly IGBT switches (with fast acting anti-parallel diodes) are used. Generally molded blocks of six switches and six diodes, connected in

bridge fashion with their power and control terminals brought out, are commercially available. These molded blocks come with isolated metallic case that need to be mounted on suitably sized heat sinks for dissipation of thermal losses in the switch. The switch manufacturers provide the turn-on and turn-off loss data for the switches for different magnitudes of dc link voltage, switch current and gate-to-emitter voltages. Similarly conduction loss data for the switches and the diodes are also provided. The thermal resistance data (thermal resistance between case and semiconductor-junction) for the switches and diodes are also provided. The heat-sink manufacturers provide data / guide lines for calculating the thermal resistance between heat sink and ambient. The inverter designer needs to do a detailed analysis of the worst-case thermal losses and temperature rise and need to limit the switch current accordingly. In PWM inverters, because of large number of switching per output cycle, the load current frequently jumps from controlled switch (say, IGBT) to diode and hence the diodes of the switches must also be rated to carry the peak magnitude of load current. It is to be kept in mind that in PWM inverters the load current polarity changes only according to the output frequency and not according to the switching frequency. For load power factor close to one, as the PWM inverter's output voltage decreases the diode conduction duration increases. The worst-case diode losses also need to be determined for deciding on the de-rating factor for diode currents.

Quiz Problems

(1) A PWM inverter is operated from a dc link voltage of 600 volts. The maximum rms line voltage (fundamental component) will be less than or equal to:
   (a) 600 volts
   (b) 300 volts
   (c) 467 volts
   (d) 582 volts

(2) In the harmonic analysis of the pole-voltage waveform (produced by a three-phase PWM inverter feeding a balanced three-phase load) the 3^{rd} and multiples of 3^{rd} harmonics are ignored because:
   (a) They will not appear in pole voltage
   (b) They will not appear in load phase voltage
   (c) They will not appear in load phase and line voltage
   (d) They will appear in line voltage but not in phase voltage

(3) An IGBT based PWM inverter, with very large number of (nearly) evenly distributed notches per output cycle, is used to feed a three-phase balanced R-L load with a load power factor of 0.9. The peak magnitude of diode current and the IGBT current will have the following relation:
   (a) They will be equal
   (b) Peak diode current will be less than half of the peak IGBT current
   (c) Diode current will nearly be zero
   (d) Peak diode current will be less than one third of the peak IGBT current

(4) A PWM inverter is capable of producing the following type of output voltage:
   (a) Variable in magnitude and frequency
   (b) Variable voltage, fixed frequency
   (c) Fixed voltage, variable frequency
   (d) Fixed voltage, fixed frequency

Answers to Quiz problems: 1-c, 2-c, 3-a, 4-a