Problems

Q1. There are 4 types of power dissipation in CMOS circuits. Since one of the major aim of VLSI design these day, in smaller Technology Nodes, is to reduce the total power consumption. We have power dissipation techniques as:

a) Static power dissipation
b) active power dissipation (dynamic)
c) Switching power dissipation
d) Leakage power dissipation (Major ones)
   i) Subthreshold leakage
   ii) Gate leakage
   iii) GIDL and
   iv) Reverse bias source (Dyain/substrate) and B to B leakage current.

In moderate Technology nodes, major power dissipation is due to dynamic power given by

\[ P = \alpha CV^2 f \]

To improve this PD to lower values one can apply with parameters: \( \alpha, V_{dd}, f \) and \( C \). But optimizing each together is very difficult for minimizing power.

Explain how then dynamic power can be minimize.

Q2. Using only Shift-Add operation, show \( m \times n \) multiplier can be used realized using Booth's algorithms. Prove, compared to other multiplier circuits, this booth kind multiplier is most efficient. Take example of two arithmetic set of numbers like \((77 \times 83)\) and \((64 \times 96)\), implement the multipliers.

Q3. An CMOS inverter (draw figures) could be symmetrical invert kind and symmetrical input signal type. If we have specs like \( \beta_n = \beta_p = \beta^{w/L} \) (w/L) and risetime and fall time \( \ell = \ell_r = \ell_f \), prove short circuits power is \( (i) \alpha \ell \ (ii) \alpha \beta (iii) V^3 \). Take some relevant values for parameters and prove above.

Q4. For Inverter shown, of take same values of parameters of components, evolution (I) switching power (ii) Energy per Transition (III) Total energy for completed time cycle
Q5. Translinear circuits are wonderful implementation of current mode MOS circuit used in Mixed-Mode circuits.

(a) Translinear loop using P-N junctions (diodes)
(b) Translinear loop of the circuit (left) implemented using composite bipolar and sub threshold MOS transistors. The loop is employed in a current conveyor configuration where the bidirectional output current $I_{out}$ equals to the bidirectional current $I_{in}$.

Here saturated current of MOS transistors realize performances of Diodes. The Diode current is expressed as

$$I_{DS} = \frac{S \cdot I_{SAs}}{\exp \left[ \frac{K \cdot (V_{GS} - V_{TH})}{q} \right]}$$

Where $S = \frac{W}{L}$ and $K$ is prefactor like $\beta \left( \frac{W}{L} \right)$ in MOS equation.

From symbols as above in fig.5, show that

$$\ln \left( \frac{I_1}{I_2} \right) = \ln \left( \frac{I_1}{I_4} \right)$$

what this imply?