1. Consider an instruction pipeline with four stages with the stage delays 5 nsec, 6 nsec, 11 nsec, and 8 nsec respectively. The delay of an inter-stage register stage of the pipeline is 1 nsec. What is the approximate speedup of the pipeline in the steady state under ideal conditions as compared to the corresponding non-pipelined implementation?
   a. 4.0
   b. 2.5
   c. 1.1
   d. 3.0

Correct answer is (b).

Time taken to execute N instructions in non-pipelined implementation will be \((5 + 6 + 11 + 8)N = 30N\)

Clock period for pipelined implementation = \(\max\{5,6,11,8\} + 1 = 12\).

Time taken for the pipelined implementation = \((3 + N)12 = 12N\) (approx.)

Speedup = \(\frac{30N}{12N} = 2.5\)

2. Consider an instruction pipeline with five stages without any branch prediction: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Operand Write (OW). The stage delays for IF, ID, OF, EX and OW are 5 nsec, 7 nsec, 10 nsec, 8 nsec and 6 nsec, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 nsec. A program consisting of 12 instructions I1, I2, ..., I12 is executed in the pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, the time needed to complete the program is:
   a. 132 nsec
   b. 154 nsec
   c. 176 nsec
   d. 328 nsec

Correct answer is (b).
Minimum clock period = \( \max\{5,7,10,8,6\} + 1 = 11 \)

I1: IF ID EX ME WB
I2: IF ID EX ME WB
I3: IF ID EX ME WB
I4: IF ID EX ME WB
I5: . . . . .
I6: . . . . .
I7: . . . . .
I8: . . . . .
I9: IF ID EX ME WB
I10: IF ID EX ME WB
I11: IF ID EX ME WB
I12: IF ID EX ME WB

Total 14 clock cycles are needed, i.e. \( 14 \times 11 = 154 \) nsec.

3. Consider a RISC machine where each instruction is 4 bytes long. Conditional and unconditional branch instructions use PC-relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Also, the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence:

Instruction i: ADD R2,R3,R4
Instruction i+1: SUB R5,R6,R7
Instruction i+2: SEQ R1,R9,R10
Instruction i+3: BEQZ R1,Offset

If the target of the branch instruction is i, the decimal value of Offset will be ...............

Correct answer is -16.

Assume that instruction "i" starts from memory address X.

Address of instruction i+1 = X + 4
Address of instruction i+2 = X + 8
Address of instruction i+3 = X + 12
Address of instruction i+4 = X + 16

So, Offset = X – (X + 16) = -16

4. A 5-stage pipelined processor has the stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Write Operand (WO). The IF, ID, OF, and WO stages take 1 clock cycle each for any instruction. The EX stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction, and 6 clock cycles for DIV instruction. Operand forwarding is used in the pipeline (for data dependency, OF stage of the dependent instruction can be executed only
after the previous instruction completes EX). What is the number of clock cycles needed to execute the following sequence of instructions?

\[
\begin{align*}
\text{MUL} & \quad R2,R10,R1 \\
\text{DIV} & \quad R5,R3,R4 \\
\text{ADD} & \quad R2,R5,R2 \\
\text{SUB} & \quad R5,R2,R6
\end{align*}
\]

a. 13  
b. 17  
c. 15  
d. 19

Correct answer is (c).

\[
\begin{align*}
\text{MUL} \ R2, R10, R1 & : \text{ IF ID OF EX EX EX WO} \\
\text{DIV} \ R5, R3, R4 & : \text{ IF ID OF EX EX EX EX EX WO} \\
\text{ADD} \ R2, R5, R2 & : \text{ IF ID - - - - - - OF EX WO} \\
\text{SUB} \ R5, R2, R6 & : \text{ IF - - - - - - ID - OF EX WO}
\end{align*}
\]

Number of clock cycles \(= 15\).

5. Consider an instruction pipeline for the MIPS32 processor where data references constitute 42\% of the instructions, and the ideal CPI ignoring memory structural hazards is 1.25. How much faster is the ideal machine without the memory structural hazard versus the machine with the hazard?

a. 1.34  
b. 1.26  
c. 1.38  
d. None of the above

Correct answer is (a).

\[
\text{Speedup} = \frac{\text{Ideal CPI} \times \text{Pipeline Depth}}{\text{Ideal CPI} + \text{Stall cycles per instr}}
\]

So, \(\text{Speedup}_{\text{ideal}} = \frac{1.25 \times \text{Depth}}{1.25 + 0} = \text{Depth}\)

And, \(\text{Speedup}_{\text{real}} = \frac{1.25 \times \text{Depth}}{1.25 + 0.42 \times 1} = 1.25 \times \text{Depth} / 1.67\)

Required answer = \(1.67 / 1.25 = 1.34\) (approx.)

6. In MIPS32 pipeline, what are the measures that can be taken to reduce the impact of data hazards?

a. Splitting the memory into separate Instruction and Data memories.  
b. Implement data forwarding in the datapath.  
c. Allow split register write and read during the two halves of the same clock cycle.  
d. Replicate the register bank.

Correct answers are (b) and (c).

Option (a) reduces the impact of structural hazard. Option (d) will also not help in mitigating data hazards.
Data forwarding and split register access can reduce the number of stall cycles.

7. In the MIPS32 pipeline, which of the following scenarios of data dependency will always result in a pipeline stall due to data hazard without any instruction scheduling?
   a. An ADD instruction followed by a SUB instruction.
   b. A STORE instruction followed by a LOAD instruction
   c. A LOAD instruction followed by an ADD instruction.
   d. None of the above.
   
   Correct answer is (c).

Only a LOAD followed by an immediate use will result in a mandatory stall in the pipeline.

8. Instruction scheduling can be used to eliminate data and control hazard by:
   a. Schedule the execution of the instruction only if there is no hazard.
   b. Allowing the compiler the move instructions around to fill the LOAD/BRANCH delay slot(s) with meaningful instructions.
   c. Using a special hardware to check for hazard and issue instructions only when possible.
   d. None of the above.

   Correct answer is (b).

Instruction scheduling is a compiler technique where instructions are moved around keeping dependencies in mind so as to reduce the wasted cycles due to stalls.

9. Consider the MIPS32 pipeline with ideal CPI of 1. Assume that 30% of all instructions executed are branch, out of which 80% are taken branches. The pipeline speedup for predict taken and delayed branch approaches to reduce branch penalties will be:
   a. 4.10 and 4.45
   b. 3.25 and 4.35
   c. 3.67 and 4.25
   d. 3.85 and 4.35

   Correct answer is (d).

For predict taken, branch penalty = 1
   Speedup = 5 / (1 + 0.30 x 1) = 3.85

For delayed branch, branch penalty = 0.5
   Speedup = 5 / (1 + 0.30 x 0.5) = 4.35

10. For the 1-bit prediction scheme, which of the following statements are false?
   a. There will be two mispredictions whenever the behavior of a branch instruction changes.
   b. An entry in the BPB uniquely identifies a branch instruction.
c. Does not give any advantage for the MIPS32 pipeline.
d. None of the above.

Correct answer is (b).

(a) is true, and also (c) is true. Since BPB stores only a few lower-order bits of the branch instruction, two different instructions can have the same values of the lower-order bits. Hence it cannot uniquely identify a branch instruction.

11. In a MIPS pipeline with Branch Target Buffer (BTB), assume that 85% of the branches are found in BTB, 10% of the predictions are incorrect, and 80% of the branches are taken. The branch penalty will be ...............clock cycles.

Correct solution is 0.44.

Branch Penalty = (% branches found in BTB x % mispredictions x 2) + (% branches not found in BTB x % taken branches x 2) + (% branches not found in BTB x % not-taken branches x 1)

= 0.85 x 0.10 x 2 + 0.15 x 0.80 x 2 + 0.15 x 0.20 x 1 = 0.44